AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please add claims 21-24.

1. (CURRENTLY AMENDED) A memory circuit comprising:

a bit cell configured to generate a bit signal having a fixed logic value;

a sense amplifier configured to generate a reset signal in response to sensing said bit signal; and

a control circuit configured to (i) set a control latch in response to a detection signal and (ii) reset said control latch in response to said reset signal, wherein said control latch is set while both said detection signal and said reset signal are in an asserted state to halt a self-timed read cycle.

2. (CURRENTLY AMENDED) The memory circuit according to claim 1, further comprising a detection circuit configured to generate said detection signal in said asserted state in response to detecting a transition of an address signal.

3. (ORIGINAL) The memory circuit according to claim 1, further comprising a pass gate configured to block said reset signal generated by said sense amplifier in response to said detection signal.

4. (CURRENTLY AMENDED) The memory circuit according to claim ~~3~~ 1, further comprising a bias circuit configured to generate said reset signal in a de-asserted state to said control circuit in response to said detection signal.

5. (ORIGINAL) The memory circuit according to claim 1, further comprising:

a pair of bit lines conveying said bit signal from said bit cell to said sense amplifier; and

a charging circuit configured to reset at least one of said bit lines in response to said detection signal.

6. (CURRENTLY AMENDED) The memory circuit according to claim 1, further comprising~~:~~

a reset latch configured to latch said reset signal as generated by said sense amplifier~~; and~~

~~a driver circuit configured to drive said reset latch to a de-asserted state in response to said detection signal~~.

7. (CURRENTLY AMENDED) The memory circuit according to claim ~~6~~ 21, wherein ~~(i)~~ said control circuit is further configured to generate an enable signal in response to said detection signal ~~and (ii) said driver circuit is further configured to drive said reset latch to said de-asserted state in response to said enable signal~~.

8. (PREVIOUSLY PRESENTED) The memory circuit according to claim 1, wherein said sense amplifier is further configured to generate said reset signal in a de-asserted state in response to said detection signal transitioning from said asserted state to said de-asserted state.

9. (CURRENTLY AMENDED) The memory circuit according to claim ~~8~~ 1, wherein said sense amplifier is further configured to start a new read of said bit cell in response to said detection signal transitioning from said asserted state to ~~said~~ a de-asserted state.

10. (ORIGINAL) The memory circuit according to claim 1, further comprising:

a pass gate configured to block said reset signal generated by said sense amplifier in response to said detection signal;

a bias circuit configured to generate said reset signal in a de-asserted state to said control circuit in response to said detection signal;

a pair of bit lines conveying said bit signal from said bit cell to said sense amplifier;

a charging circuit configured to reset at least one of said bit lines in response to said detection signal;

a reset latch configured to latch said reset signal as generated by said sense amplifier; and

a driver circuit configured to drive said reset latch to said de-asserted state in response to said detect signal.

11. (CURRENTLY AMENDED) A method of operating a memory circuit comprising the steps of:

(A) generating a bit signal having a fixed logic value;

(B) generating a reset signal in response to sensing said bit signal;

(C) setting a control latch in response to a detection signal; and

(D) resetting said control latch in response to said reset signal, wherein said control latch is set while both said detection signal and said reset signal are in an asserted state to halt a self-timed read cycle.

12. (CURRENTLY AMENDED) The method according to claim 11, further comprising the step of generating said detection signal in said asserted state in response to detecting a transition of an address signal.

13. (CURRENTLY AMENDED) The method according to claim 11, further comprising the step of blocking said reset signal ~~at a first location~~ in response to said detection signal.

14. (CURRENTLY AMENDED) The method according to claim ~~13~~ 11, further comprising the step of generating said reset signal in

a de-asserted state ~~at a second location~~ in response to said detection signal.

15. (ORIGINAL) The method according to claim 11, further comprising the steps of:

conveying said bit signal in two portions from a first location to a second location; and

resetting at least one of said portions in response to said detection signal.

16. (CURRENTLY AMENDED) The method according to claim 11, further comprising the ~~steps~~ step of:

latching said reset signal at a location~~; and~~

~~driving said reset signal to a de-asserted state at said location in response to said detection signal~~.

17. (CURRENTLY AMENDED) The method according to claim ~~16~~ 11, further comprising the ~~steps~~ step of:

generating an enable signal in response to said detection signal~~; and~~

~~driving said reset signal to said de-asserted state at said location in response to said enable signal~~.

18. (CURRENTLY AMENDED) The method according to claim 11, further comprising the step of:

generating said reset signal in a de-asserted state in response to said detection signal transitioning from said asserted state to said de-asserted state.

19. (CURRENTLY AMENDED) The method according to claim ~~10~~ 11, further comprising the step of:

starting a new read of said bit signal in response to said detection signal transitioning from said asserted state to ~~said~~ a de-asserted state.

20. (CURRENTLY AMENDED) A memory circuit comprising:

means for generating a bit signal having a fixed logic value;

means for generating a reset signal in response to sensing said bit signal;

means for setting a control latch in response to a detection signal; and

means for resetting said control latch in response to said reset signal, wherein said control latch is set while both said detection signal and said reset signal are in an asserted state to halt a self-timed read cycle.

21. (NEW) The memory circuit according to claim 6, further comprising a driver circuit configured to drive said reset latch to a de-asserted state in response to said detection signal.

22. (NEW) The memory circuit according to claim 7, wherein said driver circuit is further configured to drive said reset latch to said de-asserted state in response to said enable signal.

23. (NEW) The method according to claim 16, further comprising the step of:

driving said reset signal to a de-asserted state at said location in response to said detection signal.

24. (NEW) The method according to claim 17, further comprising the step of:

driving said reset signal to said de-asserted state in response to said enable signal.